REMARKS

Pending Claims

Claims 1 and 6 are pending. Claims 1 and 6 have been amended. No new matter has been added.

Claim Rejections Under 35 U.S.C. §103

Claims 1 and 6 are rejected under 35 U.S.C. §103(a) as being unpatentable over Dietz, "Meta-State Conversion", in view of Panchul et al, U.S. Patent Publication No. 2001/0034876, further in view of Nakata et al, "Deriving Parameter Conditions for Periodic Timed Automata Satifying Real-Time Temporal Logic Formulas".

Applicants request reconsideration of the rejections in view of the foregoing amendments and for the following reasons.

Applicants have amended independent claims 1 and 6. Claims 1 and 6 have been amended to clarify that the state allotment candidates obtained are allotted so as not to concur and a section from each state to another state is traversed by a Depth First Search. Additionally, a transition corresponding to the "sync" block is detected for the automaton and is set as a "sync" transition and the number of states is decreased by collecting into one transition, the transitions which are not successive transitions. Additionally, claim 1 has been amended to set forth that the parametric model checking is performed using the temporal automaton for the parameter generator. Support for the amendment can be found on pg 41, line 12 to pg 42, line 5 of the Specification, for example.

Dietz is relied upon in the Office Action for disclosing a meta state conversion algorithm that allows SIMD (Single Instruction stream, Multiple Data stream) hardware to efficiently support a control parallel programming model. See pg 2 of Dietz under the heading Introduction. The input language accepted by the meta state converter of Dietz is MIMDC. See pg 17, section 4.1. Each processor has its own state and it is possible to view the set of processor states at a particular time as a single meta state and a complier can convert the MIMD program into an automaton based on meta states. See pg 3, section 1.2. Further, Dietz discloses converting the code for the MIMD processes into a set of control flow graphs in which each node represents a basic block. See pge 4 section 2. Additionally, Dietz merely describes a block synchronization that prevents any transitions past a MIMD state contained in a meta state if the MIMD state is a barrier synchronization point. See pg 13, section 2.6. Further, the barrier synchronization of Dietz does not result in a runtime operation, but rather contains the asynchrony as defined by the algorithm shown on pg 13 of Dietz. See pg 14, lines 1-2.

However, Dietz does not disclose a clock boundary node, which does exist in the "sync" block, that is set as a state allotment candidate, as claimed by Applicants in claims 1 and 6. Further, Dietz does not disclose that the state allotment candidates obtained are allotted so as not to concur and a section from each state to another state is traversed by a Depth First Search, as claimed by Applicants in claims 1 and 6. Dietz is deficient in disclosing that a transition corresponding to the "sync" block is detected for the automaton and is set as a "sync" transition. Further, Dietz does not disclose decreasing the number of states by collecting into one transition, the transitions which are not successive transitions, as

claimed by Applicants in claims 1 and 6.

Panchul is relied upon for describing the facilitation of the design of an actual hardware implementation for digital circuits using a high-level programming language, such as the Java programming language. However, Panchul does not disclose inputting program descriptions as set forth in claims 1 and 6 wherein restrictions which are an inhibition of dynamic instantiation and an inhibition of a start method call from the run method are imposed on the program descriptions by employing the Java program language. Accordingly, Panchul does not overcome the deficiencies in Dietz with respect to the invention claimed in claims 1 and 6.

Nakata is relied upon for disclosing a symbolic model checking method for parametric periodic timed automata. However, Nakata does not disclose the intermediate expression claimed by applicants which comprises a temporal automaton and a concurrent control flow flag generated by expressing the start of the "synchronized" operation as a node which is labeled as "Begin sync" and the end thereof as a node which is labeled as "End sync", as set forth in claims 1 and 6.

The features of the invention, as now more clearly recited in the claims, are not taught or suggested by Dietz, Panchul, Nakata and the other cited references whether considered individually or in combination with each other in the manner suggested by the Examiner. Accordingly, claims 1 and 6 are patentable over Dietz in view of Panchul in further view of Nakata. Accordingly, Applicants request that the rejection of claims 1 and 6 under 35 U.S.C. §103(a) be withdrawn and the application allowed.

Conclusion

In view of the foregoing, Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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